DATA SHEET

TDA8808T

TDA8808AT

Photo diode signal processor for compact disc players

Product specification

File under Integrated Circuits, IC01

Philips
Semiconductors

PHILIPS

Photo diode signal processor for
compact disc players

TDA8808T
TDA8808AT

GENERAL DESCRIPTION

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

• Data amplifier with equalizer and AGC

• Offset-free pre-amplifier with AGC for the servo signals

• Trackloss and drop-out detection

• Start-up procedure for focus

• Normalizing focus error output signal to minimize radial error interference

• Laser supply amplifier and reference source

• Both TDA8808T and TDA8808AT versions suitable for car, portable and home applications

• Single and dual supply application

• Focus in-lock signal; ready signal output (RD).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Supply					
V_P	Supply voltage range		4,5	5,0	5,5	V
	External voltage range					
V_{ext}	TDA8808T		−5,5	−5,0	0	V
V_{ext}	TDA8808AT		V_P	10	12	V
I_Q	Quiescent supply current	Si/$\overline{RD}$ = 0 V	7,5	10	12,5	mA
	HF input current					
$I_{HFin(p\text{-}p)}$	(peak-to-peak value)	f_{HFin} = 100 kHz	3	–	10	µA
	LF input current					
I_D	(for each diode input)		0	–	6	µA
I_{LO}	Laser supply output current	Si/$\overline{R7D}$ = HIGH Z	−8	−4	−2	mA
	Operating ambient					
T_{amb}	temperature range		−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A); SOT136-1; 1996 August 13.

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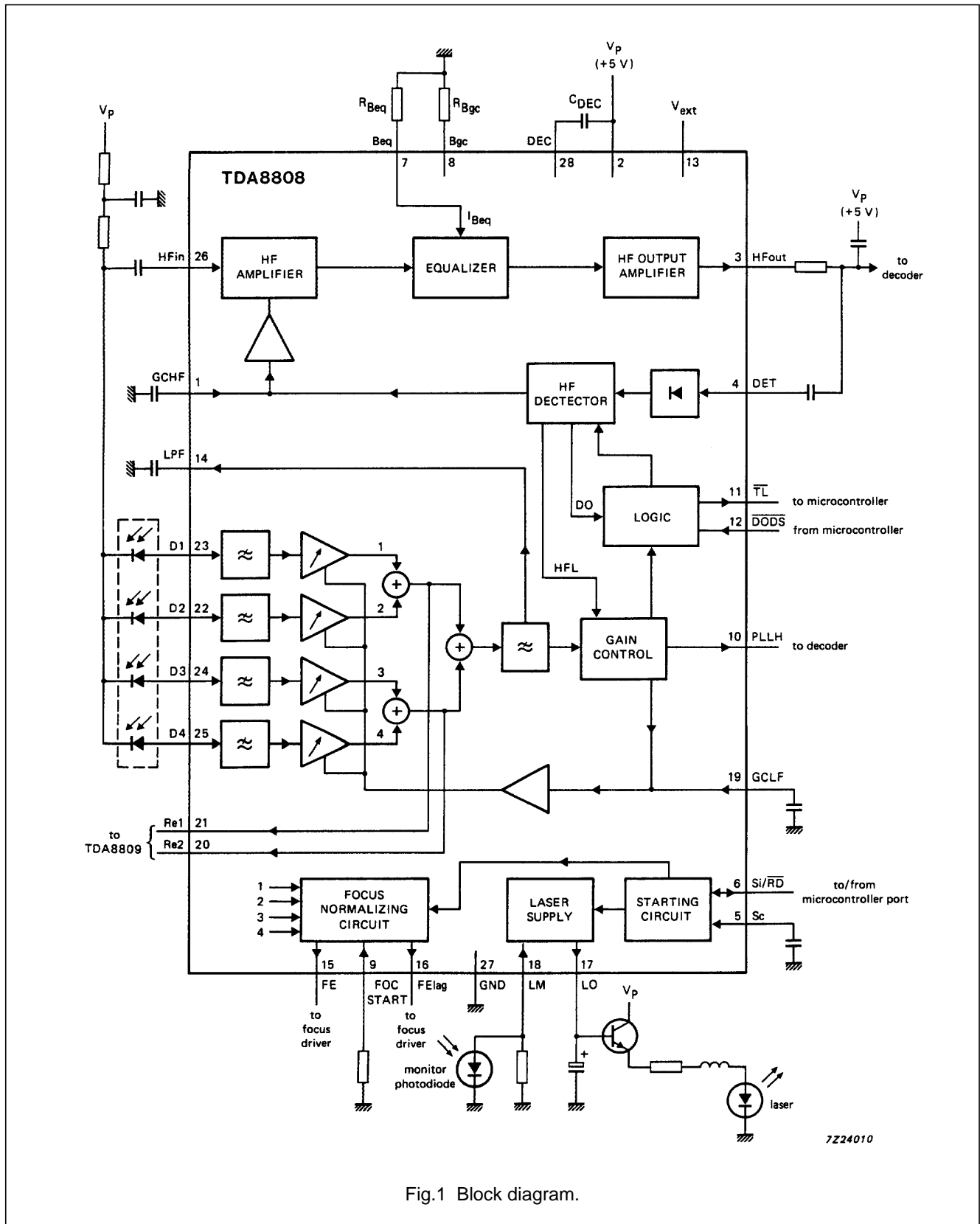disc players

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Fig.1 Block diagram.

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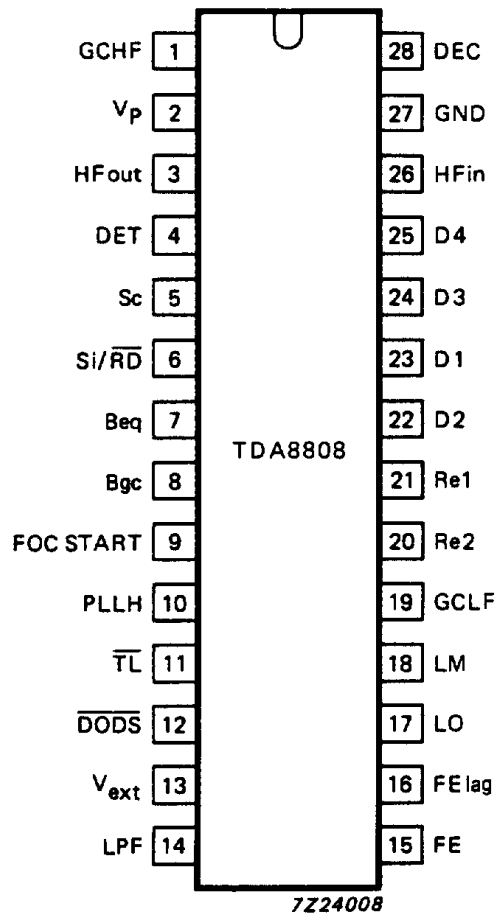
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PINNING

Fig.2 Pinning diagram.

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Pin functions

PIN	MNEMONIC	DESCRIPTION
1	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector
2	V_P	Positive supply voltage
3	HFout	HF amplifier and equalizer voltage output
4	DET	HF detector voltage input
5	Sc	Starting up capacitor input
6	Si/$\overline{RD}$	On/off control (start input); ready signal output (starting up procedure successful)
7	Beq	Equalizer reference current input
8	Bgc	DC and LF gain control reference current input
9	FOC START	Focus normalizing circuit starting current
10	PLLH	PLL on hold output
11	$\overline{TL}$	Track loss output
12	$\overline{DODS}$	Drop out detector suppression input
13	V_{ext}	TDA8808T
		Negative supply connection for FE and FElag output stage; also
		substrate connection
		TDA8808AT
		Positive supply connection for FE and FElag output stage
14	LPF	Low pass filter for I_{ret}, used in track loss ($\overline{TL}$) detector and LF gain control
15	FE	Current output of normalized, switched focus error signal
16	FElag	Current output of switched focus error signal, intended for lag network.
17	LO	Laser amplifier current output
18	LM	Laser monitor diode input
19	GCLF	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector
20	Re2	Summation of amplified currents from D3 and D4
21	Re1	Summation of amplified currents from D1 and D2
23, 22	D1, D2	Current inputs to DC and LF photo diode amplifier
24, 25	D3, D4	Current inputs to DC and LF photo diode amplifier
26	HFin	Current input to HF amplifier
27	GND	Ground connection of device: also substrate connection for TDA8808AT
28	DEC	Decoupling input (internal bypass)

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
	Supply voltage ranges (see Fig.3)			
	TDA8808T			
$V_P–V_{(ext)}$	pin 2 to pin 13	–0,3	13	V
$V_{GND}–V_{(ext)}$	pin 27 to pin 13	–0,3	13	V
	TDA8808AT			
$V_{ext}–V_{GND}$	pin 13 to 27	–0,3	13	V
$V_P–V_{GND}$	pin 2 to pin 27	–0,3	13	V
	Output voltage ranges			
V_O	except FE and FE_{lag}	0	V_P	V
V_O	FE and FE_{lag} (TDA8808T)	V_{ext}	V_P	V
V_O	FE and FE_{lag} (TDA8808AT)	V_{GND}	V_{ext}	V
V_O	LM (open loop)	V_{GND}	V_P	V
P_{tot}	Total power dissipation	see Fig.4		
T_{stg}	Storage temperature range	–55	+ 150	°C
T_{amb}	Operating ambient temperature range	–30	+ 85	°C
T_j	Operating junction temperature	–	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ =   140 K/W
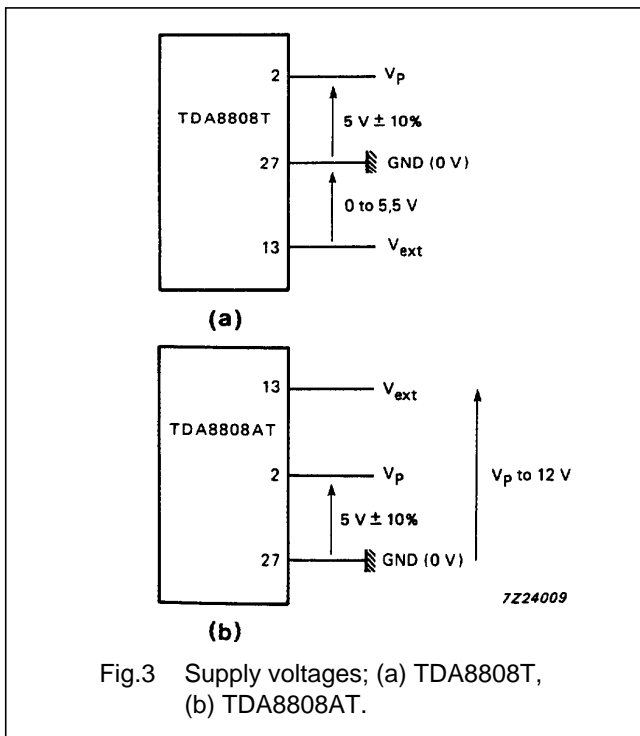

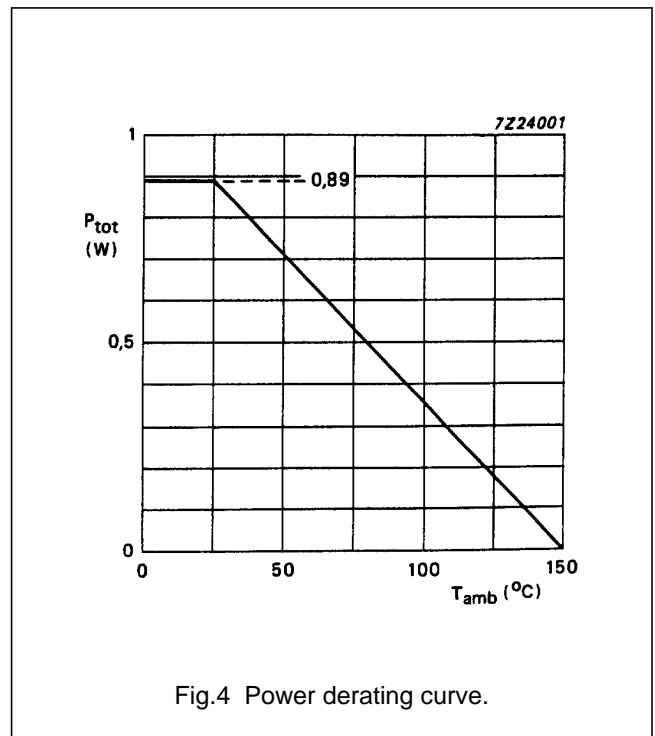Fig.3 Supply voltages; (a) TDA8808T,
(b) TDA8808AT.

Fig.4 Power derating curve.

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CHARACTERISTICS

$V_P = + 5$ V; $V_{GND} = 0$ V; $V_{ext} = -5$ V (TDA8808T); $V_{ext} = + 10$ V (TDA8808AT); $V_{RE1} = V_{RE2} = 3,5$ V; $V_{FE} = V_{FElag} = 0$ V (TDA8808T); $V_{FE} = V_{FElag} = 5$ V (TDA8808AT); $R_{FOC\ START} = 3,3$ kΩ; $I_{Beq} = I_{Bgc} = 50$ µA (current sources); $T_{amb} = 25$ °C; all voltages measured with respect to V_{GND}, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Supply					
V_P	Supply voltage range		4,5	5,0	5,5	V
	External voltage range					
V_{ext}	TDA8808T		−5,5	−5,0	0	V
V_{ext}	TDA8808AT		V_P	10	12	V
I_Q	Quiescent supply current	$V_{Si/\overline{RD}} = 0$ V	7,5	10	12,5	mA
	Reference input (Beq)					
V_{Beq}	Input voltage level		500	560	620	mV
I_{Beq}	Input current		–	−50	–	µA
	Reference input (Bgc)					
V_{Bgc}	Input voltage level		1,15	1,25	1,35	V
I_{Bgc}	Input current		–	−50	–	µA
	Decoupling input (DEC)					
V_{DEC}	Input voltage level		–	V_P−1,4	–	V
$\lvert Z_{DEC} \rvert$	Input impedance		–	2	–	kΩ
	HF input (HFin)					
V_{HFin}	Input voltage level		–	1,4	–	V
	HF input current					
$I_{HFin(p-p)}$	(peak-to-peak value)	$f_{HFin} = 100$ kHz	3	–	10	µA
$\lvert Z_{HFin} \rvert$	Input impedance		0,5	1	2	kΩ
	HF part					
	DC characteristics					
	$\text{Gain (G1)} = \dfrac{\Delta V_{HFout}}{\Delta I_{HFin}}$	$I_{HFin} = \pm 1$ µA				
G1(max)	Maximum gain	$V_{GCHF} = 4$ V	390	480	570	mV/µA
G1(min)	Minimum gain	$V_{GCHF} = 1,5$V	−5	0	5	mV/µA
	AC characteristics					
G2	$\text{Gain (G2)} = 20 \log \dfrac{V_{O1}}{V_{O2}}$	note 1	2	3,5	5	dB
G3	$\text{Gain (G3)} = 20 \log \dfrac{V_{O1}}{V_{O2}}$	note 2	4	5,5	7	dB
	Phase of input/output signal					
ϕ	at 1 MHz	note 3	–	$\pi/2$	–	rad.

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\tau 300$	Group delay at f_{HFin} = 300 kHz + Δf	note 3	–	290	–	ns
$\Delta\tau$	Flatness between 0,1 and 1 MHz	note 3	*	9	*	ns
	HF output (HFout)					
V_{HFout}	Output voltage at I_{HFin} = 0	V_{GCHF} = 4 V	1,5	2,4	3,3	V

$V_{O1(p-p)}$	Output voltage
	    (peak-to-peak value)
	    at $I_{HFin(p-p)}$ = 7 μA
		note 4	1	1,20	–	V

$V_{O(p-p)}$	at $I_{HFin(p-p)}$ = 4 to 10 μA	note 5	–20%	M_1	+20%	V
$|Z_{HFout}|$	Output impedance		–	60	–	Ω
	HF detector input (DET)	see Fig.5				
V_{DET0}	DC voltage level	I_{DET} = 0	–	2,2	–	V
V_{refp}	Positive reference voltage V_{DET} to V_{DET0}		–10%	540	+10%	mV
V_{refn}	Negative reference voltage V_{DET} to V_{DET0}		–5%	$-V_{refp}$	+5%	mV
$|Z_{DET}|$	Input impedance		–	9	–	kΩ
	Gain control (GCHF)					
V_{GCHF}	Input voltage for: minimum HF gain		–	1,8	–	V
V_{GCHF}	maximum HF gain		–	3,4	–	V
$|Z_{GCHF}|$	Input impedance at V_{GCHF} = 1,5 to 4 V		–	25	–	MΩ
I_{GCHF}	Output current (see Fig.5) $\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = LOW	90	100	110	μA
I_{GCHF}	$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = HIGH	86	96	106	μA
I_{GCHF}	$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = LOW	–0,65	–0,35	–0,2	μA
I_{GCHF}	$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = HIGH	–5,0	–4,4	–3,8	μA
I_{GCHF}	$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	$\overline{DODS}$ = X**	–0,65	–0,35	–0,2	μA
	V_{DETp1}/V_{refp}; V_{DETn1}/V_{refn}		10	12,5	15	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	PLLH output (pin 10)					
	Output voltage LOW					
V_{PLLHL}	I_{PLLH} = 400 µA (sink current)		–	–	0,4	V
	Output voltage HIGH					
V_{PLLHH}	I_{PLLH} = −50 µA (source current)		2,4	–	–	V
I_{PLLH}	Output sink current		0,5	1,5	–	mA
I_{PLLH}	Output source current		–	−100	−50	µA
I_{DT1}	Threshold total LF current	V_{GCLF} = 3,5 V	–	2,0	–	µA
	V_{DETp2}/V_{refp}; V_{DETn2}/V_{refn}		57,5	62,5	67,5	%
	LF photo diode inputs (pins 22 to 25)					
	(values given for each input)					
V_D	DC voltage level		–	1,2	–	V
I_D	Input current range		0	–	6	µA
$|Z_D|$	Input impedance at 1 MHz	I_D = 1 µA	–	10	–	kΩ
	LF gain					
	Maximum DC gain					
	for: $A_1 = \left\| \dfrac{I_{Re1}}{I_{D1} + I_{D2}} \right\|$;	V_{GCLF} = 3,5 V				
	$I_{D3} = I_{D4} = 0$					
A_{11}	at I_{D1} = 0 µA; I_{D2} = 1 µA		S_1−10%	S_1	S_1	
A_{12}	at I_{D1} = 1 µA; I_{D2} = 0 µA		S_1 or 55	S_1	S_1	
	for: $A_2 = \left\| \dfrac{I_{Re2}}{I_{D3} + I_{D4}} \right\|$;	V_{GCLF} = 3,5 V				
	$I_{D1} = I_{D2} = 0$					
A_{21}	at I_{D3} = 0 µA; I_{D4} = 1 µA		S_1−10%	S_1	S_1	
A_{22}	at I_{D3} = 1 µA; I_{D4} = 0 µA		S_1 or 55	S_1	S_1	
	S_1 mean value of					
	A_{11}, A_{12}, A_{21}, A_{22}		55	64	84	
	Minimum DC gain					
	for: $A_3 = \left\| \dfrac{I_{Re1}}{I_{D1} + I_{D2}} \right\|$;	V_{GCLF} = 0,8 V				
	$I_{D3} = I_{D4} = 0$					
A_{31}	at I_{D1} = 0 µA; I_{D2} = 1 µA		S_{2}-1	S_2	S_2+1	
A_{32}	at I_{D1} = 1 µA; I_{D2} = 0 µA		S_{2}-1	S_2	S_2+1	
	for: $A_4 = \left\| \dfrac{I_{Re2}}{I_{D3} + I_{D4}} \right\|$;	V_{GCLF} = 0,8 V				
	$I_{D1} = I_{D2} = 0$					
A_{41}	at I_{D3} = 0 µA; I_{D4} = 1 µA		S_{2}−1	S_2	S_2+1	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_{42}	at $I_{D3} = 1$ μA; $I_{D4} = 0$ μA		$S_2 - 1$	S_2	$S_2 + 1$	
	S_2 mean value of					
	A_{31}, A_{32}, A_{41}, A_{42}		$-0,1$	$0,7$	3	
	AC gain for:					
	$G_4 = 20 \log P_1$; $I_{D3} = I_{D4} = 0$					
G_4	at $I_{D1} = 0$; $I_{D2(p-p)} = 1$ μA + 2 μADC	note 6	$-4,5$	-3	$-1,5$	dB
G_4	at $I_{D1(p-p)} = 1$ μA + 2 μADC; $I_{D2} = 0$	note 6	$-4,5$	-3	$-1,5$	dB
	$G_5 = 20 \log P_2$; $I_{D1} = I_{D2} = 0$					
G_5	at $I_{D3} = 0$; $I_{D4(p-p)} = 1$ μA + 2 μADC	note 7	$-4,5$	-3	$-1,5$	dB
G_5	at $I_{D3(p-p)} = 1$ μA + 2 μADC; $I_{D4} = 0$	note 7	$-4,5$	-3	$-1,5$	dB
	Gain control (GCLF)					
	Input voltage for:					
V_{GCLF}	minimum LF gain		–	1	–	V
V_{GCLF}	maximum LF gain		–	$2,8$	–	V
$\|Z_{GCLF}\|$	Input impedance		–	25	–	MΩ
	Threshold total LF current	I_{DT3}	–	$1,6$	–	mA
	Output current (see Fig.7)					
I_{GCLF}	$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	$I_{DT} < I_{DT3}$	–	$-0,6$ I_{Bgc}	± 10	μA
I_{GCLF}		$I_{DT} > I_{DT3}$; note 8	$S_6 - 10$	S_6	$S_6 + 10$	μA
I_{GCLF}	$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$		–	$-0,2$ I_{Bgc}	± 2	μA
	Re1, Re2 outputs (pin 21, pin 20)					
	Output current	$V_{GCLF} = 3,5$ V				
I_{Re1}	at $I_{D1} = I_{D2} = 1$ μA; $I_{D3} = I_{D4} = 0$		110	128	168	mA
I_{Re1}	at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		–	0	–	mA
I_{Re2}	at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1$ μA		110	128	168	mA
I_{Re2}	at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		–	0	–	mA
	Output voltage					
V_{Re1}	pin 21		1	–	V_P	V
V_{Re2}	pin 20		1	–	V_P	V
	Output impedance					
$\|Z_{Re1}\|$	pin 21		–	1	–	MΩ
$\|Z_{Re2}\|$	pin 20		–	1	–	MΩ
	Reference current (I_{ret})					
I_{ret}	$I_{ret} = I_{Re1} = I_{Re2}$	note	200	220	240	μA
	LPF output (pin 14)					
V_{LPF}	DC voltage level	note 9	$V_P - 2,1$	$V_P - 1,7$	$V_P - 1,4$	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Z_{LPF} \rvert$	Input impedance		–	3	–	kΩ
	FOC START input (pin 9)					
	Start current (ST) for FE					
I_{ST}	($-I_{FOC\ START} = I_{ST}$)	Si/$\overline{RD}$ = HIGH Z	75	150	500	µA
I_{ST}		Si/$\overline{RD}$ = LOW	–	0	–	µA
	Start voltage (ST) for FE					
V_{ST}	($V_{FOC\ START} = V_{ST}$)	Si/$\overline{RD}$ = HIGH Z	430	530	630	mV
V_{ST}		Si/$\overline{RD}$ = LOW	–20	0	20	mV
	FElag output (pin 16)	see Fig.8				
	Output voltage					
V_{FElag}	TDA8808T		$V_{ext}+I,5$	–	$V_P-1,5$	V
V_{FElag}	TDA8808AT		+1,5	–	$V_{ext}-1,5$	V
$\lvert Z_{FElag} \rvert$	Output impedance		–	8	–	MΩ
	Output current	Si/$\overline{RD}$ = HIGH Z; V_{GCLF} = 3,5 V				
$I_{FElag}=I_O$	$I_{D1} = I_{D2} = 1_{D3} = I_{D4} = 1$ µA	$V_{Sc} = V_P$	–10	0	+10	µA
I_{FElag}	$I_{D2} = I_{D3} = 1$ µA; $I_{D1} = I_{D4} = 2$ µA	$V_{Sc} = V_P$	–10%	$-2S_1 +I_O$	+10%	µA
I_{FElag}	$I_{D2} = I_{D3} = 2$ µA; $I_{D1} = I_{D4} = 1$ µA	$V_{Sc} = V_P$	–10%	$-2S_1 +I_O$	+10%	µA
I_{FElag}	$I_{D2} = I_{D3} = 2$ µA; $I_{D1} = I_{D4} = 1$ µA	V_{Sc} = 1,5 V	–5	0	+5	µA
I_{FElag}	$I_{D2} = I_{D3} = 1$ µA; $I_{D1} = I_{D4} = 2$ µA	V_{Sc} = 1,5 V	–5	0	+5	µA
	FE output (pin 15)	see Fig.8				
	Output voltage					
V_{FE}	TDA8808T		$V_{ext}+1,5$	–	$V_P-1,5$	V
V_{FE}	TDA8808AT		+1,5	–	$V_{ext}-1,5$	V
$\lvert Z_{FE} \rvert$	Output impedance		–	8	–	MΩ
	Output current	note 10				
I_{FE}	$I_{D1} = I_{D4} = 2$ µA; $I_{D2} = I_{D3} = 1$ µA	$V_{Sc} = 0$	–10%	$-2S_1-134-I_{ST}$	+10%	µA
I_{FE}	$I_{D1} = I_{D4} = 1$ µA; $I_{D2} = I_{D3} = 2$ µA	$V_{Sc} = 0$	–10%	$-4S_1-67-I_{ST}$	+10%	µA
I_{FE}	$I_{D1} = I_{D4} = 2$ µA; $I_{D2} = I_{D3} = 1$ µA	V_{Sc} = 1,25 V	–10%	$-2S_1-134+I_{ST}$	+20%	µA
I_{FE}	$I_{D1} = I_{D4} = 1$ µA; $I_{D2} = I_{D3} = 2$ µA	V_{Sc} = 1,25 V	–10%	$-4S_1-67+I_{ST}$	+20%	µA

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I_{FE}	$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1{,}75$ V	-20%	$-2S_1+67+I_{ST}$	$+10\%$	μA
I_{FE}	$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1{,}75$ V	-10%	$-4S_1-67+I_{ST}$	$+20\%$	μA
$I_{FE} = S_6$	$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = V_P$	-20%	67	$+20\%$	μA
I_{FE}	$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = V_P$	-15%	$-S_6$	$+15\%$	μA
I_{FE}	$I_{D1} = I_{D2} =$ $I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	-10	0	$+10$	μA
I_{FE}	$I_{D1} = I_{D2} =$ $I_{D3} = I_{D4} = 0$	$V_{Sc} = V_P$	-5	0	$+5$	μA
	$\overline{DODS}$ logic input (pin 12)					
	Switching levels					
$V\overline{DODS}$	input voltage LOW		$-$	$-$	$+0{,}8$	V
$V\overline{DODS}$	input voltage HIGH		$+2$	$-$	$-$	V
$\overline{IDODS}$	Input source current		-35	-25	-15	μA
	Starting input (Sc)	see Fig.9				
V_{Sc}	Output voltage	$Si/\overline{RD} = $ LOW	$-$	0	$-$	V
V_{Sc}	Output voltage	$S1/\overline{RD} = $ HIGH Z	$-$	$-$	$V_P-0{,}5$	V
$\|Z_{Sc}\|$	Output impedance		$-$	*	$-$	$M\Omega$
I_{Sc}	Output source current	$Si/\overline{RD} = $ HIGH Z; $V_{Sc} = 1{,}5$ V	$-1{,}2$	-1	$-0{,}8$	μA
I_{Sc}	Output sink current	$Si/\overline{RD} = $ LOW	$0{,}5$	$1{,}2$	$2{,}0$	mA
	$Si/\overline{RD}$ logic input/output (pin 20)	see Fig.9				
$V_{Si/\overline{RD}}$	Voltage 'forced LOW'	$I_{Si/\overline{RD}} = 400\ \mu A$; $V_{Sc} = 2{,}5$ V; $V_{GCLF} < 2{,}8$ V	$-$	$0{,}15$	$0{,}4$	V
	Switching levels					
$V_{Si/\overline{RD}}$	input voltage LOW		$-$	$-$	$+0{,}8$	V
$V_{Si/\overline{RD}}$	input voltage HIGH Z	$I_{Si/\overline{RD}} = -5\ \mu A$	$2{,}4$	$2{,}8$	$-$	V
$I_{Si/\overline{RD}}$	Input source current LOW		-35	-25	-15	μA
	$\overline{TL}$ logic output (pin 11)	see Fig.6				
$V_{\overline{TL}}$	Output voltage level LOW	$I_{\overline{TL}} = 400\ \mu A$; (sink current)	$-$	$0{,}15$	$0{,}4$	V
$V_{\overline{TL}}$	Output voltage level HIGH	$I_{\overline{TL}} = -50\ \mu A$; (source current)	$2{,}4$	$-$	$-$	V

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</div>

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Threshold total LF current	I_{DT2}	–	3,9	–	µA
	Output voltage	DODS = HIGH (≥ 2,4 V)				
$V_{\overline{TL}}$	$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	2,4	–	–	V
$V_{\overline{TL}}$	$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	I_{DT} don't care	2,4	–	–	V
$V_{\overline{TL}}$	$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	2,4	–	–	V
$V_{\overline{TL}}$	$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	–	0,15	0,4	V
	Output voltage	$\overline{DODS}$ = LOW (≤ 0,8 V)				
$V_{\overline{TL}}$	$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	2,4	–	–	V
$V_{\overline{TL}}$	$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	2,4	–	–	V
$V_{\overline{TL}}$	$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	–	0,15	0,4	V
$I_{\overline{TL}}$	Output sink current	$V_{\overline{TL}}$ = LOW	1	2,2	–	mA
$I_{\overline{TL}}$	Output source current	$V\overline{TL}$ = HIGH	–	–100	–50	µA
τ1	Delay times (see Fig.10)		7	8,5	10	µs
τ2		see Fig.6	τ1–15% or 6,5	–	τ1+ 5% or 10	µs
τ3			7	8,5	10	µs
τ4			τ3–10% or 7	–	τ3+10% or 10	µs
	LO output (pin 17)					
V_{LO}	Output voltage		–	–	V_P - 0,5	V
$|Z_{LO}|$	Output impedance		–	95	–	kΩ
I_{LO}	Output leakage current	Si/$\overline{RD}$ = LOW	–10	–0,1	0	µA
I_{LO}	Maximum output current	Si/$\overline{RD}$ = HIGH Z	–8	–4	–2	mA
	LM input (pin 18)					
V_{LM}	Input voltage	closed loop	185	205	225	mV
I_{LM}	Input bias current		–2	–	–	µA
	Laser supply					
	Transconductance					
G_{LDC}	For DC (note 11)	Si/$\overline{RD}$ = HIGH Z	–	0,5	–	A/V
G_{LDC}		Si/$\overline{RD}$ = LOW	–	0	–	A/V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
τLO	For AC (note 12) delay time		–	*	–	ns

    *   Value to be fixed.

    **   X = don't care.

Notes to the characteristics

1. Voltage output signal V_{O1} measured at f_{HFin} = 700 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.

2. Voltage output signal V_{O1} measured at f_{HFin} = 1 MHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.

3. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p-p)}$ = 1 μA; V_{GCHF} = 4 V.

   $$\text{Group delay } \tau = \frac{d\phi}{dw} \; ; \Delta f \approx 50 \text{ kHz.}$$

   Flatness: $\Delta\tau = \tau_{max} - \tau_{min}$.

4. HF part output voltage for closed loop conditions; f_{HFin} = 500 kHz.

5. HF part output voltage for closed loop conditions; f_{HFin} = 0,1 to 1 MHz.
   M_1 is the measured value of V_{O1}.

6. P_1 is the measured value of $\dfrac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \dfrac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$

   Where: (1) are the current levels at f_i = 25 kHz.
                 (2) are the current levels at f_i = 1 kHz.
   Measurement taken at V_{GCLF} = 3,5 V.

7. P_2 is the measured value of $\dfrac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \dfrac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$

   Where: (1) are the current levels at f_i = 25 kHz.
                 (2) are the current levels at f_i = 1 kHz.
   Measurement taken at V_{GCLF} = 3,5 V.

8. S_6 is the measured value of $S_1 \cdot \dfrac{I_{DT}}{4} - 1, 1 \; I_{Bgc}$

   Measurement taken at V_{GCLF} = 3,5 V.

9. LF part reference current I_{ret} and low-pass filter output voltage for closed loop conditions.
   Measurement taken at $I_{DT} > I_{DT3;} \Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$.

10. FE output current measured at $V_{GCLF} = 3, 5 \text{ V and } Si/\overline{RD} = HIGH \; Z; \; I_{ST} = \dfrac{V_{FOC\;START}}{R_{FOC\;START}}$

11. Laser supply transconductance for DC

    $$G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}} \; (0 < -I_{LO} < 2 \text{ mA})$$

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12. Laser supply transconductance for AC

$$G_{LAC} = G_{LO} \cdot \frac{1}{1 + S \cdot \tau LO}$$
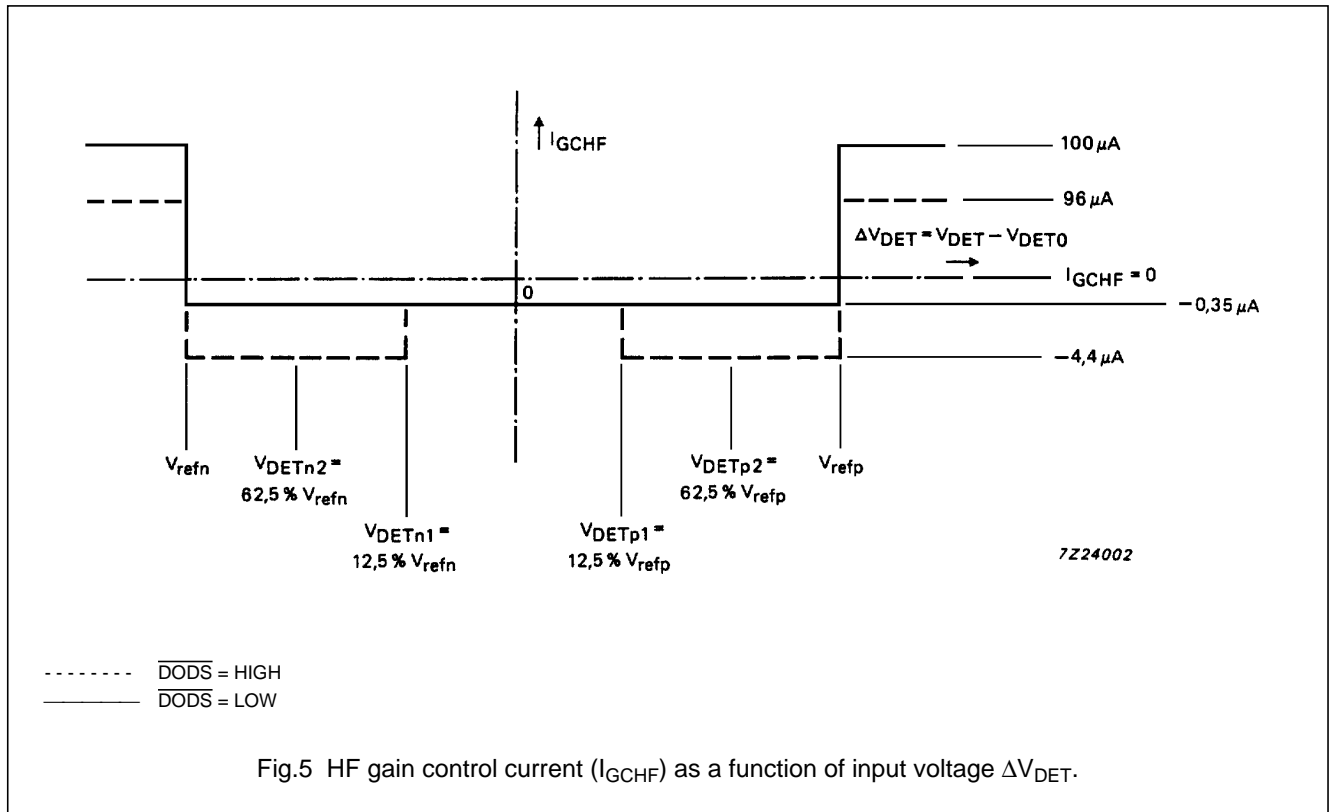
Where: S is the laplace operator in the frequency domain.

Fig.5 HF gain control current (I_{GCHF}) as a function of input voltage ΔV_{DET}.

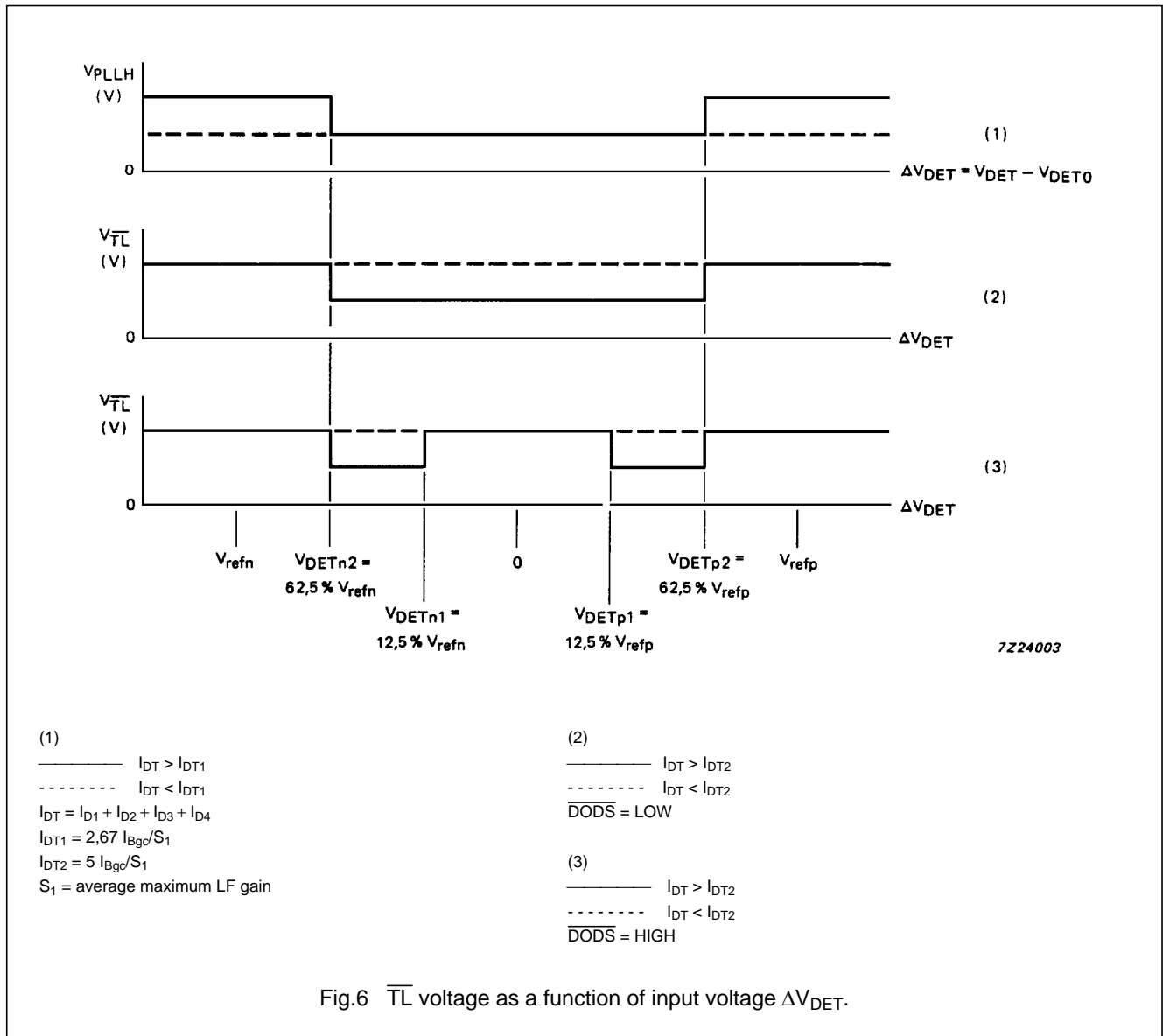## Photo diode signal processor for compact disc players

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(1)

——————— $I_{DT} > I_{DT1}$
- - - - - - - - $I_{DT} < I_{DT1}$
$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$
$I_{DT1} = 2{,}67\ I_{Bgc}/S_1$
$I_{DT2} = 5\ I_{Bgc}/S_1$
S_1 = average maximum LF gain

(2)

——————— $I_{DT} > I_{DT2}$
- - - - - - - - $I_{DT} < I_{DT2}$
$\overline{DODS}$ = LOW

(3)

——————— $I_{DT} > I_{DT2}$
- - - - - - - - $I_{DT} < I_{DT2}$
$\overline{DODS}$ = HIGH

Fig.6　$\overline{TL}$ voltage as a function of input voltage ΔV_{DET}.

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$V_{DETn2} = 62,5\% \, V_{refn}$

$V_{DETp2} = 62,5\% \, V_{refp}$

$I_{GCLF} = 0$

$S_1 \times \dfrac{I_{DT}}{4} - 1{,}1 \, I_{Bgc}$

$-0{,}2 \, I_{Bgc}$

$-0{,}6 \, I_{Bgc}$

7Z24004

- - - - - - - $I_{DT} > I_{DT3}$

───────── $I_{DT} < I_{DT3}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT3} = 2 \, I_{Bgc}/S_1$

S_1 = average maximum LF gain

Fig.7 LF gain control current (I_{GCLF}) as a function of input voltage ΔV_{DET}.

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I_{ST} = $-I_{FOC\ START}$

I_{cont} = $2 I_{Bgc}$ if $I_{DT} > I_{DT3}$

I_{cont} = $I_{DT} \times S_1$ if $I_{DT} < I_{DT3}$

I_{DT} = $I_{D1} + I_{D2} + I_{D3} + I_{D4}$

I_{DT3} = $2 I_{Bgc}/S_1$

S_1 = average maximum LF gain

$(1 + 4)NN$ = not normalized currents = $(I_{D1} + I_{D4}) S_1$

$(2 + 3)NN$ = not normalized currents = $(I_{D2} + I_{D3}) S_1$

$(1 + 4)\ N$ = normalized currents = $\left(\dfrac{I_{D1}}{I_{D1} + I_{D2}} + \dfrac{I_{D4}}{I_{D3} + I_{D4}} \right) \times I_{cont}$

$(2 + 3)\ N$ = normalized currents = $\left(\dfrac{I_{D2}}{I_{D1} + I_{D2}} + \dfrac{I_{D3}}{I_{D3} + I_{D4}} \right) \times I_{cont}$

V_j is the junction voltage (0,7 V typ.).

Fig.8 FElag current output as a function of starting voltage input (V_{Sc}).

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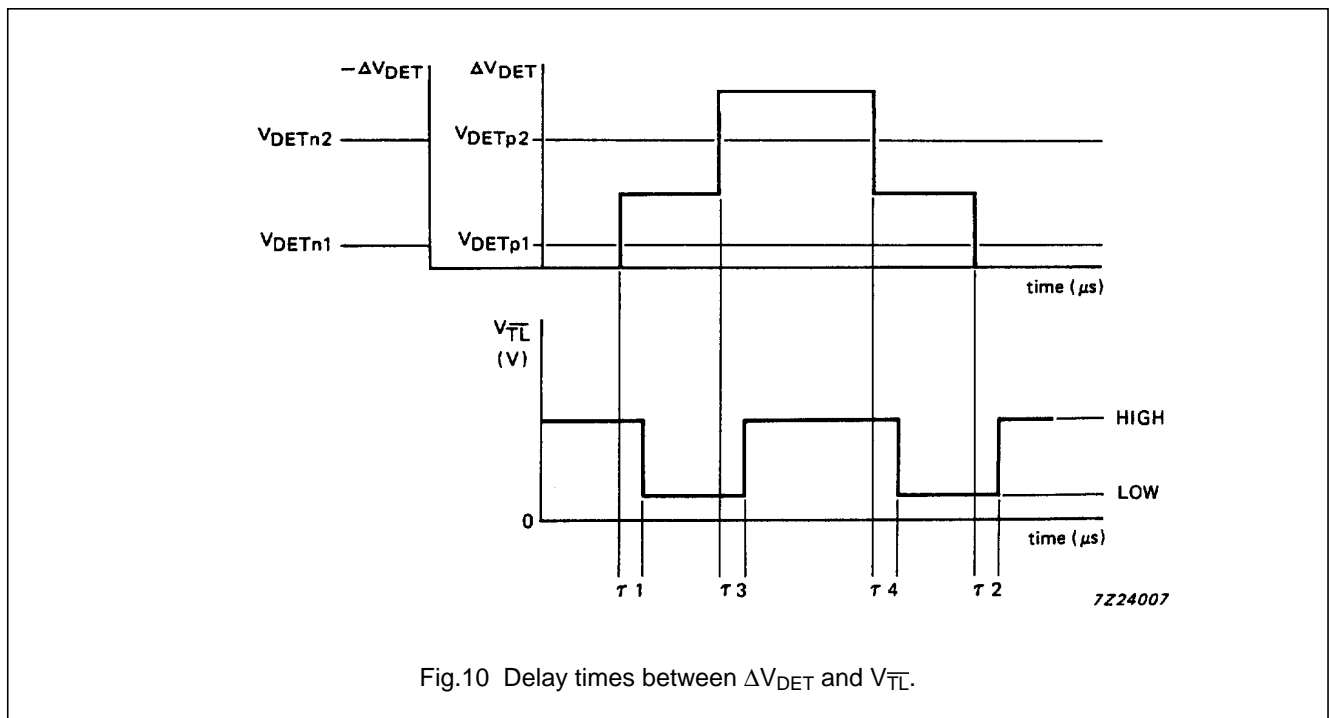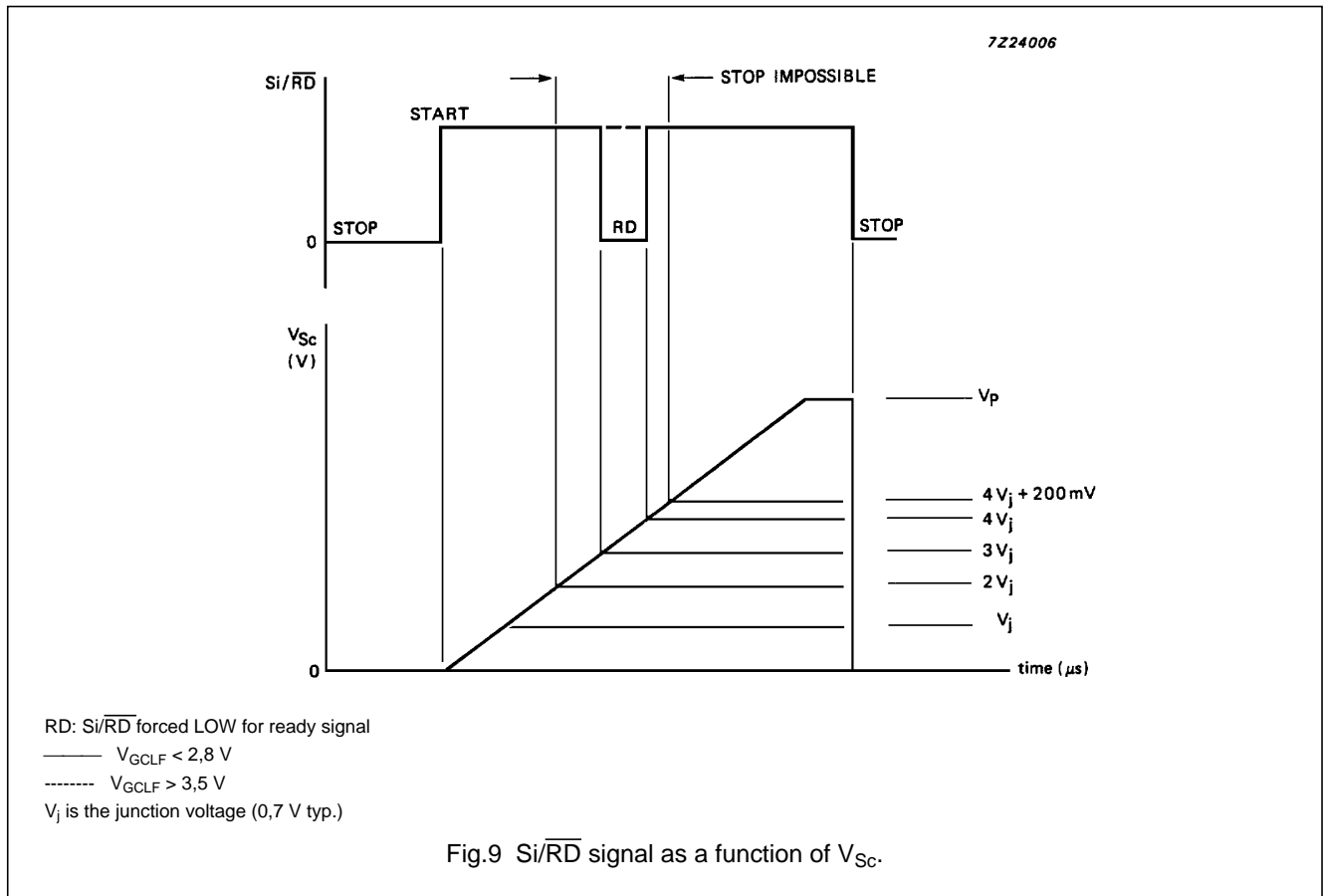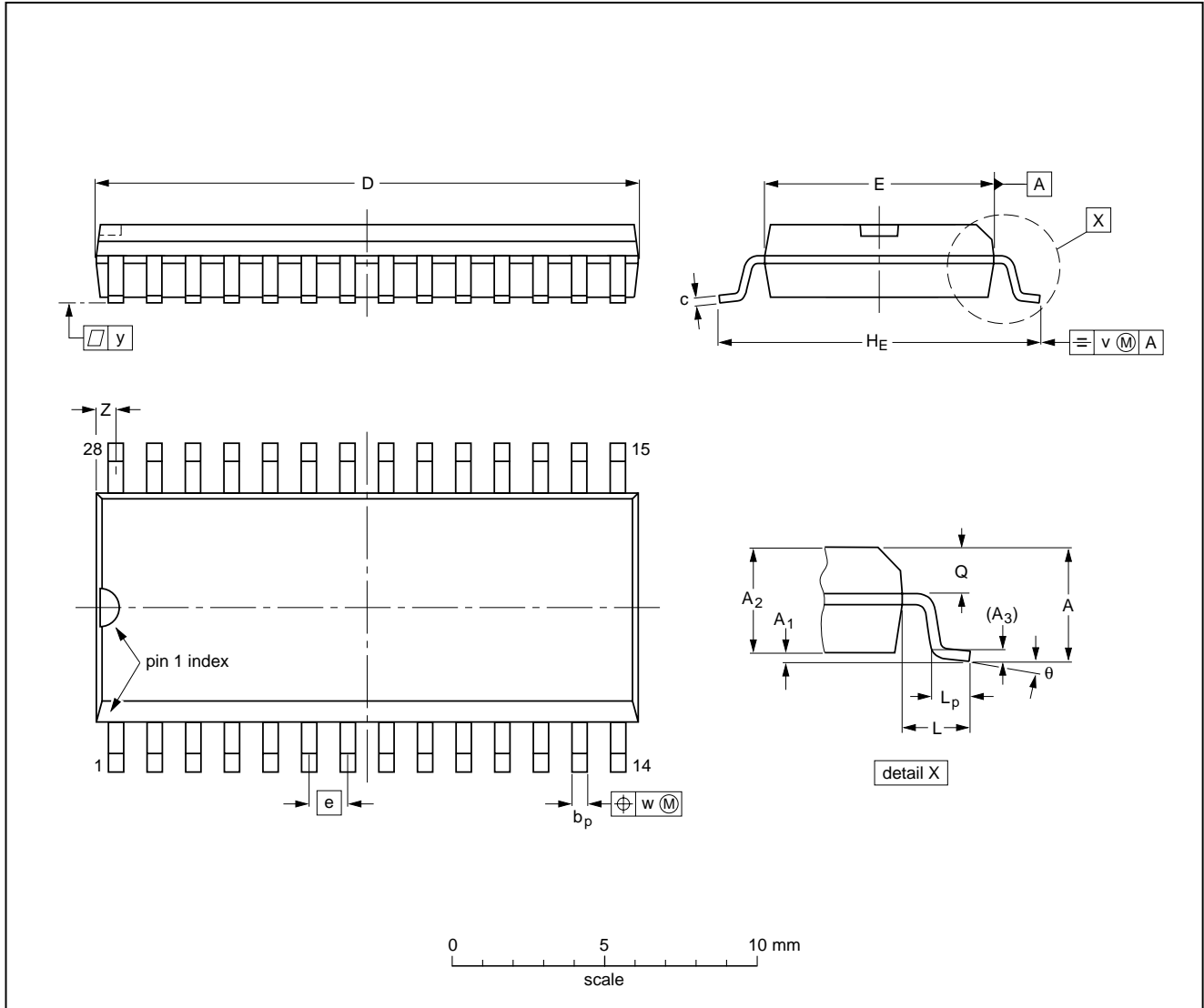disc players

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RD: Si/$\overline{\text{RD}}$ forced LOW for ready signal

———— $V_{GCLF} < 2,8$ V

-------- $V_{GCLF} > 3,5$ V

V_j is the junction voltage (0,7 V typ.)

Fig.9 Si/$\overline{\text{RD}}$ signal as a function of V_{Sc}.

Fig.10 Delay times between ΔV_{DET} and $V_{\overline{TL}}$.

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PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm

SOT136-1

pin 1 index

detail X

scale
0   5   10 mm

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				95-01-24 97-05-22

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 $^{\circ}$C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 $^{\circ}$C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.

- The longitudinal axis of the package footprint must be parallel to the solder flow.

- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 $^{\circ}$C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 $^{\circ}$C within 6 seconds. Typical dwell time is 4 seconds at 250 $^{\circ}$C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 $^{\circ}$C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 $^{\circ}$C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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